

## Description

# FOUR-PHASE DUAL PUMPING CIRCUIT

### BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention generally relates to charge pumps, and more particularly, to methods and apparatus for generating a high positive or a negative voltage for memory devices.

[0003] 2. Description of the Prior Art

[0004] The era of digital information has arrived which pushed the development of electronic information processing devices such as computers, wireless devices, personal digital assistants (PDAs), portable multimedia players/recorders, and the like in the recent years. One crucial component to any electronic information processing device is the memory device which has gone under substantial advancement. The performance in speed and reliability along with the size and packaging of these memory devices have greatly improved as a result smaller and faster memory



devices are continuously being introduced to the market.

[0005] In order to reduce power consumption and extend battery life, much of the integrated circuitry such as memory devices used in portable devices is being designed to run at low voltage levels. This reduces the power usage and reduces the heat generated by the circuit components allowing more components to be placed closer to one another. The circuitry and components used in portable computers typically are being designed to operate at voltages levels substantially less than the previous standard of 5V, with 1.0V and lower becoming increasingly common.

[0006] A major problem is that conventional charge pumps have difficulty dealing with the lower battery voltages being used. In particular, the MOS transistors used in the charge pumps have switching threshold voltages that are a large fraction of the supply voltage. The problem is related to the fact that diode-connected transistors develop increasing back-bias between the source and the body of the transistor as the voltage increases along the length of the pump. The result of this back-bias (also known as the "source-body effect", "M factor", or "body effect") is to increase the effective threshold of the transistor, in some



higher voltage cases almost doubling it. With increased effective transistor thresholds and decreased supply voltages, the charge pump transistors would no longer switch properly and the charge pump would not work.

[0007] Many designs used a technique called "bootstrapping" to generate higher amplitude clock signals to compensate for the increased effective threshold voltages relative to the supply voltage. The bootstrapping technique involves the use of a charge capacitor that charges on every clock pulse and discharges between pulses, adding the discharged voltage to the original input voltage of the bootstrapping circuit so the output could be multiplied to a number of times the original input. Applying a uniform high clock voltage, generated by bootstrapping, leads to energy inefficiency because the greater the current delivered by the clocking voltage, the less efficient the bootstrapping operation. In the latter stages where high voltages are required, this inefficiency was unavoidable. In the initial stages of the charge pump, where as high a voltage is not needed, the clock bootstrapping operation was inefficient.

[0008] In general, currently available charge pumps are inefficient, large, and complex. They do not properly deal with



low initial supply voltages and fail to address the problems inherent with higher threshold voltages caused by the body effect. A solution, which would provide a simple charge pump with efficient operation using a low initial supply voltage, has long been sought but has eluded those skilled in the art. As the popularity grows of portable battery-powered devices in which such a design could be particularly useful, it is becoming more pressing that a solution be found.

[0009] Different approaches to designing charge pumps were previously disclosed. "Charge pump circuit having a boosted output signal" U.S. Patent Number 4,935,644 by J.Tsujimoto shown in FIG. 1 and 2 discloses a charge pump circuit having a first charge pump circuit and a second charge pump circuit that is controlled by two phase clocks. The first and the second charge pump circuits comprise a series of serially diode-connected MOSFETs where the gates of the transistors in the second charge pump are connected to the corresponding stage transistors in the first charge pump. The final output of the first charge pump circuit is connected to a high resistance element so there is no external loss and the second charge pump circuit can achieve an adequate boost-up voltage



where there is a greater external current loss. Tsujimotos charge pump circuit uses two identical but out-of-phase clocks and no substrate connection. "Method and apparatus for a two phase bootstrap charge pump" U.S. Patent Number 5,462,469 by Tedrowshown in FIG. 3 and 4 discloses a two phase bootstrap charge pump that uses four complicated and non-identical clock signals to pre-charge the gates and transfer charge to the next stage. Tedrows two phase bootstrap charge pump does not have any substrate connection to remove body effects and uses NMOS for positive pump.

#### **SUMMARY OF INVENTION**

[0010] It is therefore a primary objective of the claimed invention to provide four-phase dual pumping circuits that provide a high positive voltage that is above the supply voltage and at the same time a high negative voltage that is lower than the ground voltage which are required for write and erase operations in memory devices to solve the above-mentioned problem.

[0011] It is another objective of the claimed invention to provide four-phase dual pumping circuits that efficiently generates the required high positive and high negative voltages using the same triple-well technology at a low supply



voltage.

- [0012] It is another objective of the claimed invention to provide a four-phase dual pumping circuit that minimizes the body effect of the main pass transistors so the output voltage is maximized.
- [0013] It is another objective of the claimed invention to provide a four-phase dual pumping circuit that avoids p-n junction conduction.
- [0014] According to the claimed invention, a four-phase dual pumping circuit is provided that can both operate as either a negative or positive dual pumping circuit. The negative dual pumping circuit uses NMOS transistors and the positive dual pumping circuit uses PMOS transistors. The dual pumping circuit of the present invention has a number of stages according to the required output voltage based on an input voltage. Each stage has a first pumping unit and a second pumping unit that are mirror and identical to each other and electrically coupled to each other, where each stage is electrically coupled to the preceding and subsequent stages. The first pumping unit and the second pumping unit of each stage generate outputs Vout1 and Vout2 respectively which are used as inputs for the subsequent stages for pumping the input voltage to a



required output voltage. The first pumping unit and the second pumping unit of each stage has a main pass transistor, a boosting transistor, and a substrate transistor, where the main pass transistor is used to transfer charge to the subsequent stage, the boosting transistor is used to pre-charge the current stage, and the substrate transistor is used to supply a high voltage to the body of the control and boosting transistors during charge transfer to reduce body effects, wherein the main pass transistor, boosting transistor, and substrate transistor have a source, drain, gate, and body terminal. The substrate transistor of either pump circuit is controlled by a high voltage signal sent from the other pump circuit. As a result the first pumping unit and the second pumping unit of each stage alternately perform the pre-charge and charge transfer operation. The operation of the dual pumping circuit of the present invention is controlled by four sets of clock pulses in which one pair of clock pulses is out of phase and one pair of clock pulses may be generated by a high voltage circuit. One clock pulse from each pair (i.e. together two) is used to control each pumping circuit of the dual pumping circuit in an alternating manner. The output of the final stage is cross-coupled to maximize the output volt-



age. Additionally the input voltage of the final stage can be cross-coupled to increase the amplitude of the input voltage.

[0015] According to the claimed invention, a method for the first stage of the dual pumping circuit is provided which includes supplying an input voltage to the source terminals of the main pass transistors of the first pumping unit and the second pumping unit; during interval one to three, the first pumping unit performs charge sharing while the second pumping unit performs pre-charge; in interval one, rendering the main pass transistors of the first pumping unit and the second pumping unit, the substrate transistor of the second pumping unit, and the boosting transistor of the first pumping unit off, and the substrate transistor of the first pumping unit and the boosting transistor of the first pumping unit on; following in interval two, rendering the main pass transistor of the first pumping unit, the substrate transistor of the first pumping unit, and the boosting transistor of the second pumping unit on, and the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off; and continuing in interval three, rendering the main pass



transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off, the boosting transistor of the second pumping unit, and the substrate transistor of the first pumping unit on.

[0016] During intervals four to six, the second pumping unit performs charge sharing while the first pumping unit performs pre-charge; in interval four, rendering the substrate transistor of first pumping unit, the main pass transistor of the first pumping unit, the main pass transistor of the second pumping unit, the boosting transistor of the second pumping unit off, and the boosting transistor of the first pumping unit, and the substrate transistor of the second pumping unit on; following in interval five, rendering the main pass transistor of the second pumping unit, the substrate transistor of the second pumping unit, and the boosting transistor of the first pumping unit on, and the substrate transistor of the first pumping unit, the main pass transistor of the first pumping unit, and the boosting transistor of the second pumping unit off; and continuing in interval six, rendering the main pass transistor of the second pumping unit, the substrate transistor



of the first pumping unit, the main pass transistor of the first pumping unit, and the boosting transistor of the second pumping unit off, and the substrate transistor of the second pumping unit and the boosting transistor of the first pumping unit on.

[0017] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

#### **BRIEF DESCRIPTION OF DRAWINGS**

[0018] FIG. 1 is a diagram of a charge pump circuit according to prior art.

[0019] FIG. 2 is a diagram of clock signals for the charge pump circuit in FIG. 1 according to prior art.

[0020] FIG. 3 is a diagram of a two phase bootstrap charge pump according to prior art.

[0021] FIG. 4 is a diagram of clock signals for the two phase bootstrap charge pump in FIG. 3 according to prior art.

[0022] FIG. 5 is a schematic circuit layout for the positive dual pumping circuit according to one embodiment of the present invention.

[0023] FIG. 6 is a magnified view of the schematic circuit layout



for the positive dual pumping circuit according to one embodiment of the present invention.

[0024] FIG. 7 is a diagram showing the clock pulses for controlling the operation of the positive dual pumping circuit in FIG. 5.

[0025] FIG. 8–13 are diagrams showing the different stages of the positive dual pumping circuit of the present invention according to the intervals of the clock pulses in FIG. 7.

[0026] FIG. 14 is a schematic diagram of the high voltage circuit of the dual pumping circuit of the present invention.

[0027] FIG. 15 is a schematic circuit layout for the negative dual pumping circuit according to one embodiment of the present invention.

[0028] FIG. 16 is a magnified view of the schematic circuit layout for the negative dual pumping circuit according to one embodiment of the present invention.

[0029] FIG. 17 is a diagram showing the clock pulses for controlling the operation of the negative dual pumping circuit in FIG. 15.

[0030] FIG. 18 is a schematic diagram showing the structure of a NMOS transistor used for the negative dual pumping circuit in FIG. 15.

[0031] FIG. 19 is a schematic diagram showing the structure of a



PMOS transistor used for the positive dual pumping circuit in FIG. 5.

[0032] FIG. 20 is a graph showing the simulated results of the positive dual pumping circuit of the present invention.

[0033] FIG. 21 is a graph showing the simulated results of the negative dual pumping circuit of the present invention.

#### **DETAILED DESCRIPTION**

[0034] Please refer to FIG. 5 which shows the circuit design of the dual pumping circuit according to one embodiment of the present invention. The dual pumping circuit is suitable for many different electrical devices and the focus of the embodiments will be on memory devices which are well known to those skilled in the art. Positive dual pumping circuit 500 comprising a plurality of PMOS, shown in FIG. 5, is illustrated with 4 stages, wherein each stage is further described in details in FIG. 8–13 where the operation of each stage is described. The dual pumping circuit 500 shown in this embodiment is exemplified by a four-phase four-stage positive charge dual pumping circuit but the number of phases and stages is not limited to what is disclosed by the present invention and can be altered according to the spirit of the present invention.

[0035] The dual pumping circuit 500 comprises four serially



linked stages 510, 520, 530, and 540 for achieving the required output voltage  $V_{out}$  from a low supply voltage  $V_{dd}$ . The positive dual pumping circuit 500 uses PMOS transistors based on triple-well with p-substrate technology which differs slightly that the negative dual pumping circuit 1500 that uses NMOS transistors. The stages 510, 520, 530, and 540 are all identical and each stage is comprised of a mirror structure further comprising an identical pair of a first pumping unit 512 and a second pumping unit 514. The first pumping unit 512 and the second pumping unit 514 of each stage are respectively electrically coupled to the first pumping unit and the second pumping unit of the preceding and subsequent stages with the exception that the first stage 510 of the dual pumping circuit is electrically coupled to an input voltage  $V_{dd}$  which is further electrically coupled to an inverter and the last stage 540 of the dual pumping circuit is electrically coupled to an output stage 550. The output  $V_{out}$  of the dual pumping circuit is electrically coupled to an output capacitor  $C_L$  and is cross-coupled so that the charge can be transferred to the output more efficiently.

[0036] Four set of clock pulses labeled  $F_a$ ,  $F_b$ ,  $F_c$ , and  $F_d$  control the operation of the dual pumping circuit 500 wherein  $F_a$



and Fc are regular clock pulses and Fb and Fd may be high voltage clock pulses generated by a high voltage circuit (HVC) which is further described in FIG. 14. The four sets of clock pulses work simultaneously to control both the first pumping unit 512 and the second pumping unit 514 of each stage.

[0037] Please continue to refer to FIG. 6 which shows another embodiment of the present invention with the addition of an extra voltage controller 601 comprising a NMOS transistor 602, a capacitor 604, and an inverter 606. The NMOS transistor 602 is controlled by an additional set of control clock pulses Fe. The additional control clock pulse Fe is set to high before the operation of the dual pumping operation and is then set to low during the operation of each stage of the dual pumping operation to prevent any P-N junction forward conduction. The NMOS transistor 602 is electrically coupled to a common node which is further electrically coupled to the capacitor 604 and the inverter 606 that are also controlled by the clock pulse Fe. The voltage controller 601 is separately electrically coupled to all stages 510, 520, 530, and 540 to ensure appropriate bias conditions at the initial pumping operation. Since the voltage controller 601 of each stage 510, 520,



530, and 540, are the same, the first voltage controller 601 of the first stage 510 is chosen to represent the rest of the duplicated stages. The voltage controller 601 is electrically coupled to the body of the main pass transistor of the first pumping unit 512 and the second pumping unit 514 to eliminate any body effect because the voltage difference of the source/drain and the body is close to zero. After the input voltage  $V_{dd}$  controlled by clock pulse  $\Phi_e$  is inputted to the first stage 510 of the dual pumping circuit 500, the transistor M1 of the first pumping unit 512 and M1o of the second pumping unit 514 (either transistor M1 or M1o being the first to transfer charge depending on the design of the clock pulses) is ready to transfer the pre-charge across to the subsequent stage 520. At the instance when the charge is transferred, the clock pulse  $\Phi_e$  is set to low and the body of the main pass transistor M1 is at  $V_{dd}$  which minimizes body effects because the voltage difference of the source/drain and the body is approximately zero. For the subsequent stages, the output from every stage is commonly electrically coupled to the voltage controller of the subsequent stages so the partially pumped output voltage from each stage is used as the voltage to control the main pass transistors of



the subsequent stages so the voltage difference of the source/drain and the body of all the subsequent stages is close to zero.

[0038] Please refer to FIG. 7 which shows the sets of clock pulses  $\Phi_a$ ,  $\Phi_b$ ,  $\Phi_c$ , and  $\Phi_d$  used to control the PMOS transistors of each stage of the dual pumping circuit in FIG. 5 of the present invention. It can be clearly identified from the diagram that the clock pulses  $\Phi_a$  and  $\Phi_c$  are out-of-phase clock pulses and clock pulses  $\Phi_b$  and  $\Phi_d$  follow clock pulses  $\Phi_a$  and  $\Phi_c$  respectively by a narrower low voltage period. The identical but out-of-phase clock pulses only require a clock generator (not shown) which reduces the cost and difficulty of design. Clock pulse  $\Phi_b$  follows clock pulse  $\Phi_a$  and clock pulse  $\Phi_d$  follows clock pulse  $\Phi_c$ . The detailed cumulative operation of all the clock pulses  $\Phi_a$ ,  $\Phi_b$ ,  $\Phi_c$ , and  $\Phi_d$  is further explained in FIG. 8–13 in conjunction with the PMOS transistors of the dual pumping circuit of the present invention. The operation of the first stage (for example) starts when the first falling edge of the clock pulse  $\Phi_a$  occurs that triggers the following pre-charge and charge transfer operations. The two consecutive falling edges between the clock pulse  $\Phi_a$  represents one period which is  $1/f$ . Within one period, there are six



intervals which are numbered 1 to 6 which are used to sequentially describe the operation of the positive dual pumping circuit FIG. 8-13 at each interval.

[0039] Please sequentially refer to FIG. 8-13 which show the operation of one exemplary stage of the dual pumping circuit of the present invention. In FIG. 8-13, each stage of the dual pumping circuit comprises a first pumping unit 802 and a second pumping unit 804 which are identical to each other and mirrored along an imaginary line  $i$  (shown only for explanation). The first pumping unit 802 comprises a first main pass PMOS transistor 812, a first boosting PMOS transistor 814, a first substrate PMOS transistor 816, a first small capacitor 818, and a first large capacitor 820. Similarly the second pumping unit comprises a second main pass PMOS transistor 822, a second boosting PMOS transistor 824, a second substrate PMOS transistor 826, a second small capacitor 828, and a second large capacitor 830. The first and the second pumping units alternately perform charge sharing which indicates that either pair of the clock pulses  $F_a$  and  $\Phi_b$  or  $\Phi_c$  and  $\Phi_d$  remains unchanged while the other pair of the clock pulses revert from high to low and vice versa within a time span of half a period. The pair of clock pulses  $\Phi_a$



and  $\Phi_b$  is used to control the first pumping unit 802 and the pair of clock pulses  $\Phi_c$  and  $\Phi_d$  is used to control the second pumping unit 804. During intervals 1–3, the first pumping unit 802 performs charge sharing while the second pumping unit performs pre-charge and during intervals 4–6, the second pumping unit 804 performs charge sharing while the first pumping unit performs pre-charge.

[0040] FIG. 8 shows the operation of the stage 530 of the dual pumping circuit 500 in FIG. 5 in interval 1 in FIG. 7 when the clock pulse  $\Phi_a$  goes from high to low, the clock pulse  $\Phi_b$  is high, the clock pulse of  $\Phi_c$  goes from low to high, and the clock pulse  $\Phi_d$  is high. As mentioned above that the first and the second pumping unit take turns to perform charge sharing and pre-charge, in intervals 1–3 only the first pumping unit 802 performs a charge sharing and the second pumping unit 804 remains in the pre-charge state. This preferred order in this embodiment is a design choice by the inventor and does not impose any restriction on the dual pumping circuit where the second pumping unit 802 can perform charge sharing first.

[0041] In interval 1, in the first pumping unit, the clock pulse  $\Phi_b$  is at high so the gate of the first main pass transistor 812 is raised and is off but the clock pulse  $\Phi_a$  goes from high



to low so the first large capacitor is not charged. The first substrate transistor 816 is turned on so the high voltage from the source of the second boosting transistor 824 in the second pumping unit 804 is transferred to the body of the first and second main pass transistors 812 and 822. At this instant, the source of the first main pass transistor 812 is high but the drain of the first main pass transistor 814 is low because the gate of the first main pass transistor 812 is raised. The first main pass transistor 814 is in an off state ready for charge sharing in the subsequent interval 2.

[0042] While the first pumping unit 802 is getting ready to perform charge sharing, the second pumping unit 804 performs pre-charge. In the second pumping unit 804, the clock pulse  $\Phi_c$  goes from low to high and clock pulse  $\Phi_d$  is at high and the second small capacitor 828 is charged and the large capacitor 830 is not charged. The second boosting transistor 824 is turned on from receiving the clock pulse  $\Phi_a$  that is at low to allow the source and drain of the second boosting transistor 824 to be in conduct to send the high voltage to the gate of the second main pass transistor 822. At the same time, the clock pulse  $\Phi_c$  that is at high raises the gate of the second substrate transis-



tor 826 so it is off. The high voltage from the clock pulse  $\Phi_d$  at high renders the second main pass transistor 822 off so the second pumping unit 804 remains in pre-charge state.

[0043] Please proceed to FIG. 9 which shows the operation of the stage 530 of the dual pumping circuit 500 in FIG. 5 in interval 2 in FIG. 7 when the clock pulse  $\Phi_a$  is low, the clock pulse  $\Phi_b$  goes from high to low, the clock pulse of  $\Phi_c$  is high, and the clock pulse  $\Phi_d$  is high. Since there is no change in the clock pulses  $\Phi_c$  and  $\Phi_d$  during intervals 1–3, the second pumping unit 804 maintains in pre-charge state and will be not be further discussed until it changes to perform charge sharing in intervals 4–6.

[0044] In this embodiment for a positive dual pumping circuit, the body of the transistors performing charge sharing is pumped to the highest voltage. In interval 2, in the first pumping unit 802, the body potentials of all the first main pass transistor 812, the first boosting transistor 814, and the first substrate transistor 816 are high when the gate of the first main pass transistor 812 receives the clock pulse  $\Phi_b$  that is at low. At this instant, the voltage from the preceding stage along with the clock pulse  $\Phi_c$  is transferred to the current stage. The first main pass tran-



sistor 812 experiences small influence of threshold voltage  $V_t$  drop because the gate voltage of the first main pass transistor 812 is much lower than its drain and source voltages. In the mean time, the voltage difference between the body, source, and drain is close to zero during the charge transfer which minimizes body effects and maximizes the gain from each stage of the dual pumping circuit of the present invention because the voltage level of the body of the transistors in the first pumping unit 802 is at the highest.

[0045] Please proceed to FIG. 10 which shows the operation of the stage 530 of the dual pumping circuit 500 in FIG. 5 in interval 3 in FIG. 7 when the clock pulse  $\Phi_a$  is low, the clock pulse  $\Phi_b$  goes from low to high, and the clock pulse of  $\Phi_c$  and  $\Phi_d$  are high. In interval 3, the state of the transistors in the first pumping unit 802 is identical to that in interval 1. Quickly after the charge sharing, the clock pulse  $\Phi_b$  rises back to high to raise the gate of the first main pass transistor 812. The first main pass transistor 812 is off. As a result, the charge at the drain and the gate are equalized for reducing threshold voltage  $V_t$  drop and body effects.

[0046] Please proceed to FIG. 11 which shows the operation of



the stage 530 of the dual pumping circuit 500 in FIG. 5 in interval 4 in FIG. 7 when the clock pulse  $\Phi_a$  goes from low to high, the clock pulse  $\Phi_b$  is at high, the clock pulse  $\Phi_c$  goes from high to low, and the clock pulse  $\Phi_d$  is at high. The operation of the stage 530 of the dual pumping circuit 500 in intervals 4–6 is a reverse operation of that in intervals 1–2 where the first pumping unit 802 is in pre-charge state and the second pumping unit 804 performs charge sharing. Since the clock pulse  $\Phi_a$  and  $\Phi_c$  are exactly out of phase and one of each is used to control the first pumping unit 802 and the second pumping unit 804, the operation of the first pumping unit 802 and the second pumping unit 804 is exactly opposite. Furthermore due to the mirror structure of the dual pumping circuit, the first pumping unit 802 is structurally identical to the second pumping unit 804 and therefore the operation of the first pumping unit 802 and the second pumping unit 804 is also a flip along the imaginary line  $i$ .

[0047] Please proceed to FIG. 12 which shows the operation of the stage 530 of the dual pumping circuit 500 in FIG. 5 in interval 5 in FIG. 7 when the clock pulse  $\Phi_a$  is high, the clock pulse  $\Phi_b$  is high, the clock pulse  $\Phi_c$  is low, and the clock pulse  $\Phi_d$  goes from high to low. Similar to interval 2,



the second pumping unit 804 performs a charge sharing while the body of the transistors in the second pumping circuit 804 are pumped to the highest level to prevent any body effects.

[0048] Please proceed to FIG. 13 which shows the operation of the stage 530 of the dual pumping circuit 500 in FIG. 5 in interval 6 in FIG. 7 when the clock pulse  $\Phi_a$  is high, the clock pulse  $\Phi_b$  is high, the clock pulse  $\Phi_c$  is low, and the clock pulse  $\Phi_d$  goes from low to high. Charge sharing by the second pumping circuit is completed and the pumped voltage is sent to the subsequent stage for further pumping.

[0049] Please refer to FIG. 14 which shows the HVC used for generating high voltage clock pulses from a low input voltage. The input voltage  $V_{in}$  is inputted to a first inverter 1402 and then to a second inverter 1404 where the voltage signal is transferred to both a first capacitor 1406 to a third inverter 1408 that is further electrically coupled to a second capacitor 1416. The first capacitor 1406 is electrically coupled to the source of the first NMOS transistor 1410 and the gate of the transistor 1412 and the second capacitor 1416 is electrically coupled to the source of the second NMOS transistor 1412 and the gate of the first NMOS



transistor 1410. As a result, the two NMOS transistors 1410 and 1412 are cross-coupled to increase the amplitude of the input voltage  $V_{in}$ . To substantially reduce body effects, the body of the third PMOS transistor 1414 is electrically coupled to the drain of a fifth NMOS transistor 1424 whose source is electrically coupled to  $V_{dd}$  and gate is controlled by clock pulse  $\Phi_e$  which also at the same time control the third capacitor 1420 through a inverter 1422. The high voltage clock pulses  $\Phi_b$  and  $\Phi_d$  can be achieved by such cross-coupling scheme to increase the pumping gain at low supply voltage and to reduce power consumption and chip area.

[0050] Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology,



the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.

[0051] Please continue to refer to FIG. 16 which shows another embodiment of the present invention with the addition of an extra voltage controller 1601 comprising a PMOS transistor 1602 and a capacitor 1604 and an inverter 1606. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted.

[0052] Please refer to FIG. 17 which shows the sets of clock pulses  $\Phi_a$ ,  $\Phi_b$ ,  $\Phi_c$ , and  $\Phi_d$  used to control the NMOS transistors of each stage of the dual pumping circuit in FIG. 15 of the present invention. It can be clearly identified from the diagram that the clock pulses  $\Phi_a$  and  $\Phi_c$  are out-of-phase clock pulses and clock pulses  $\Phi_b$  and  $\Phi_d$  follow clock pulses  $\Phi_a$  and  $\Phi_c$  respectively by a narrower high voltage period. The identical but out-of-phase clock pulses only require a clock generator (not shown) which reduces the cost and difficulty of design. Clock pulse  $\Phi_b$  follows clock pulse  $\Phi_a$  and clock pulse  $\Phi_d$  follows clock pulse  $\Phi_c$ . The detailed cumulative operation of all the



clock pulses  $F_a$ ,  $\Phi_b$ ,  $\Phi_c$ , and  $\Phi_d$  was explained previously referencing the positive circuit of FIG. 5 (see FIG. 8–13), the negative circuit having analogous operation.

[0053] Please refer to FIG. 18 and 19 which show the triple-well structure which is suitable for both NMOS and PMOS transistors in the dual pumping circuit of the present invention. The triple-well structure MOSFET with p-substrate technology is well known for those skilled in the art and will not be described in the details. FIG. 18 shows a NMOS transistor that is used in the negative dual pumping circuit in FIG. 15 and FIG. 19 shows a PMOS transistor that is used in the positive dual pumping circuit in FIG. 5. The NMOS transistor in FIG. 18 has a bias voltage of the n-well to the supply voltage  $V_{dd}$ . In FIG. 19, the voltage difference between the n-well and the source and drain of the PMOS transistor is close to zero so the threshold voltage is minimized having a  $V_{tp}$  of  $-0.89V$  and body effect is eliminated.

[0054] Please refer to FIG. 20 which shows the simulated result of the positive dual pumping circuit of the present invention having 4 stages using a supply voltage of  $1.65V$  with a loading of  $500pF$ . The graph shows three cases which are the best case, typical case, and worst case.



[0055] Please refer to FIG. 21 which shows the simulated result of the negative dual pumping circuit of the present invention having 4 stages using an input voltage of 1.65V with a loading of 500pF. The graph shows three cases which are the best case, typical case, and worst case.

[0056] In contrast to the prior art, the present invention provides a dual pumping circuit that can be implemented in either positive or negative with provides good pumping performance at low supply voltage (1V to 2V) using the popular triple-well technology. The dual pumping circuit uses four-phase clocks that has one pair of identical but out of phase clocks. The other two of the clocks may be chosen to be generated by a high voltage circuit to provide better pumping at low voltage. The positive dual pumping circuit uses PMOS transistors and the negative pumping circuit uses NMOS transistors where the transistors have special substrate connection to avoid body effect and p-n junction conduction.

[0057] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended



claims.